IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

BESANG INC.,	§	
	§	
Plaintiff,	§	
	§	
v.	§	
	§	NO. 2:23-CV-00028-JRG-RSP
MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS, LLC,	§	
	§	
Defendants.	§	

CLAIM CONSTRUCTION ORDER

BeSang Inc. alleges infringement by Micron Technology, Inc., and two of its affiliates (together, "Micron") of claims from U.S. Patent 7,378,702. Compl., Dkt. No. 1. The patent "relates to a semiconductor substrate combined with a relatively thin add-on semiconductor layer in which various vertically oriented memory elements are fabricated." '702 Patent at 1:16–19.

The parties dispute the scope of two terms from four claims. First, the parties dispute the scope of "stackable add-on layer" in Claim 13. Second, they dispute the meaning of "SOI pillar" in Claims 14–16. Having considered the parties' briefing, along with arguments of counsel at a July 22, 2025 hearing, the Court resolves the disputes as follows.

I. BACKGROUND

Generally, the patent relates to the number of circuits on chips. Traditionally, integrated circuits were "implemented on a single major surface of a substrate, such as a semiconductor wafer." '702 Patent at 1:29–30. But because these integrated circuits use a significant amount of area, chip manufacturers began making three-dimensional circuits. *Id.* at 1:30–35.

The ’702 Patent incorporates, claims priority to, and claims the benefit of U.S. Patent 7,052,941. ’702 Patent at [63], 1:7–10. Figure 1 (below) of the ’941 Patent shows a prior-art example of a three-dimensional integrated circuit. That prior art forms each of the IC layers by separate processing, and each IC layer has a semiconductor substrate (201, 203) on which devices are mounted. Generally, the devices share an electrically common substrate (241, 242) or well (243). *See generally* ’941 Patent at 1:13–52.

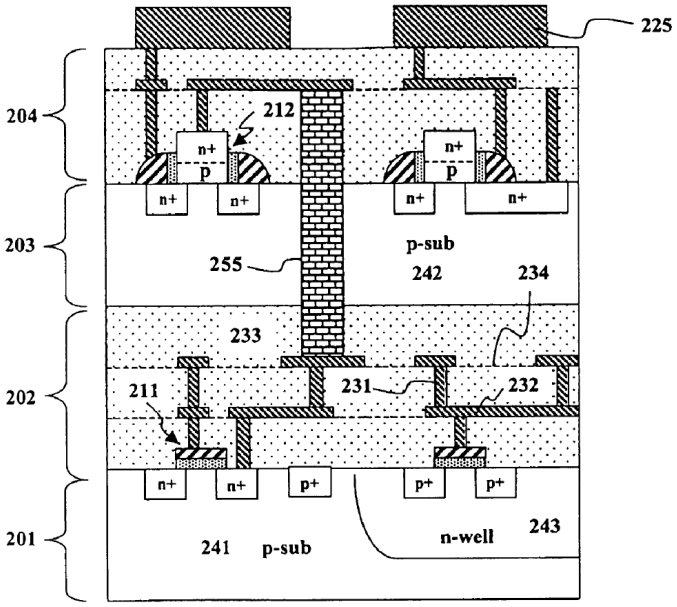

FIG. 1 of U.S. Patent 7,052,941, which is prior art

The ’702 Patent suggests a need for “structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller” relative to the prior art. ’702 Patent at 1:40–43. The patent summarizes the invention as adding “vertically oriented semiconductor memory devices, or cells, . . . to a separately fabricated substrate that includes electrical devices and/or interconnect lines.” *Id.* at 1:47–50. The patent explains this can be done in at least two ways—either (1) adding the devices to a separately fabricated substrate as a thin layer and, after adding the layer to the base substrate, etching to produce

individual doped stack structures, or (2) forming the devices in a stackable add-on layer for use in conjunction with the separately fabricated substrate. *Id.* at 1:57–2:9.

The parties' disputes concern Claims 13–16, which recite:

> 13. A semiconductor memory structure, comprising:
>
> a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
>
> a **stackable add-on layer** having a plurality of vertically oriented semiconductor memory cells; and
>
> the **stackable add-on layer** being bonded to the dielectric layer; and
>
> wherein the memory cells are nonvolatile memory cells having at least one transistor.
>
> 14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a **SOI pillar**.
>
> 15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a **SOI pillar**.
>
> 16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first **SOI pillar**.

'702 Patent at 12:24–47 (disputed terms in bold). Specifically, the parties dispute the scope of "stackable add-on layer" in Claim 13 and the meaning of "SOI pillar" in Claims 14–16.

II. LEGAL STANDARDS

"[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). As such, if the

parties dispute the scope of the claims, the court must determine their meaning. *See, e.g.*, *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007) (Gajarsa, J., concurring in part); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff'g,* 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, "is not an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, "[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims . . . ." *Id.* A court need not "repeat or restate every claim term in order to comply with the ruling that claim construction is for the court." *Id.*

When construing claims, "[t]here is a heavy presumption that claim terms are to be given their ordinary and customary meaning." *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore "look to the words of the claims themselves . . . to define the scope of the patented invention." *Id.* (citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.,* as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313. This "person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, "the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves

little more than the application of the widely accepted meaning of commonly understood words." *Phillips,* 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) ("We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history."). But for claim terms with less-apparent meanings, courts consider "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." *Phillips*, 415 F.3d at 1314.

III. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the technology, and the education of workers active in the field. *Id.* Importantly, "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Here, the parties do not dispute the level of ordinary skill. BeSang's expert opines a skilled artisan at the time of invention "would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent." Glew Decl., Dkt. No. 113-2 ¶ 20. Micron does not dispute this characterization, which the Court generally adopts to resolve the present disputes. The Court, however, limits the amount of experience to two

years.

IV. THE DISPUTED TERMS

A. "stackable add-on layer" ('702 Patent, Claim 13)

BeSang's Construction	Micron's Construction
Plain and ordinary meaning; no construction necessary. Alternative: "a layer that can be arranged in a stack and positioned above the substrate"	"a layer formed separately from the substrate suitable to be bonded to the dielectric layer positioned above the substrate"

Claim 13 recites "a stackable add-on layer . . . bonded to [a] dielectric layer." '702 Patent at 12:29–32. The parties dispute whether the recited "stackable add-on layer" excludes "a layer formed *in situ* by sequential deposition directly above the substrate." Dkt. No. 122 at 8. BeSang says there is no such exclusion and asserts no need for construction of this term. Dkt. No. 113 at 6. In its view, "the claimed layer is sufficiently defined by its role in the context of the entire claim—a layer that is arranged in a stack and positioned above the substrate." *Id.* at 7. Thus, that the layer is in a stack means it is "stackable," regardless of how it was formed. Besang also points to extrinsic evidence, including Micron documents, that it says supports its position by using the "same or similar terminology." *Id.* at 9–10.

In response, Micron says BeSang's approach reads out "stackable add-on" by converting it to "stacked." Dkt. No. 122 at 8. According to Micron, the specification consistently uses the phrase to describe a layer formed separately from the substrate. *Id.* Moreover, the specification distinguishes between "stackable add-on layers" and sequential deposition. *Id.* at 13 (citing '941 Patent at 1:53–62, 6:7–17).

The Court agrees with Micron. Although BeSang presumes anything in a "stack" must be "stackable," the specification consistently uses "stackable add-on" with reference to formation of

the layer on a separately fabricated substrate—that is, a different substrate than the "substrate" recited in Claim 13. *See, e.g.*, '702 Patent at 2:4–9 (noting DRAM, SRAM, non-volatile memory cells, and similar structures "may be formed in a stackable add-on layer for use in conjunction with the *separately fabricated substrate*" (emphasis added)), 4:48–4:53 ("'SOI layer' [refers] to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to *another previously fabricated wafer*, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer *and* the previously fabricated wafer or similar type of substrate." (emphasis added)), 4:53–57 (referring to the "stackable add-on layer" as an "attachment layer . . . suitable for bonding to a semiconductor substrate already containing devices or interconnections")); *see also id.* at [57] ("[v]ertically oriented semiconductor memory cells are added to a separately fabricated substrate").

BeSang makes four main arguments in opposition to Micron's construction, but they are not persuasive. First, BeSang says Micron's construction reads out embodiments by excluding "sequential deposition processing techniques all together" and limiting the claim to just one embodiment. Dkt. No. 113 at 17–18. BeSang, however, doesn't explain *how* Micron's construction imposes such an exclusion. Instead, BeSang points to statements made by Micron allegedly taking that position, which at most is simply Micron's argument about the scope of its construction.

Micron doesn't really take that position anyway. For example, BeSang points to a footnote in Micron's IPR appeal brief in which it agrees with the Board that "stackable add-on layer" "does not encompass sequential deposition." Dkt. No. 113 at 17 (quoting Micron's Appeal Br., Dkt. No. 113-21 at 18 n.2). But the Board simply said *bonding* the "stackable add-on layer" to the dielectric layer excludes sequential deposition—not that *formation* of the "stackable add-on layer" *prior to bonding* excludes sequential deposition. *See* Final Judgment, Dkt. No. 122-3 at 12 ("[W]e

understand that a 'stackable add-on layer' is a layer that is formed separately from the substrate and then bonded to the dielectric layer positioned above the substrate."); *see also* Micron's IPR Petition, Dkt. No. 113-6 at 6 n.2 (asserting "the intrinsic record does not support any interpretation of Claim 13 that encompasses *forming the "stackable add-on layer"* by sequential deposition directly on the substrate" (emphasis added)). And to remove any doubt, in this proceeding Micron explains its construction "simply requires a 'stackable add-on layer' to be formed separately from the substrate—without restriction on how it is formed—such that it is suitable to be bonded to the dielectric layer positioned above the substrate." Dkt. No. 122 at 24.

Second, BeSang says Micron's construction introduces method steps into a structural claim. Dkt. No. 113 at 19. But Micron's construction refers to structure formed a certain way, not the step of forming that structure. At most, this might make the claim akin to a product-by-process claim. *See Amgen Inc. v. F. Hoffmann-La Roche, Ltd.*, 580 F.3d 1340, 1370 (Fed. Cir. 2009) ("In determining infringement of a product-by-process claim, however, the focus is on the process of making the product as much as it is on the product itself."). Regardless, the applicant—not Micron—used this claim language and wrote this specification to give the term this meaning.

Third, BeSang says Micron's construction is inconsistent with the extrinsic evidence. Dkt. No. 113 at 21. BeSang stresses "Micron's own engineers and materials use the same or similar terminology to refer to Micron's 3D NAND structures produced by sequential deposition processes." *Id.* at 22. The Court, however, finds nothing in BeSang's extrinsic evidence that refers to a "stackable add-on layer," so while it's technically true the materials "use the same *or* similar terminology," it's really just "similar terminology." Regardless, extrinsic evidence cannot trump the meaning given by the intrinsic record. *See Key Pharms. v. Hercon Labs. Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998) (disapproving "attempt[s] to use extrinsic evidence to arrive at a claim

construction that is clearly at odds with the claim construction mandated by . . . the written record of the patent").

Fourth, BeSang suggests the word "separately" in "separately fabricated" throughout the specification refers to time rather than space. In other words, BeSang suggests the substrate of the prior art would be "separately fabricated" because it is fabricated before any sequential deposition on the substrate. Thus, in BeSang's view, the patent's frequent reference to a "separately fabricated substrate" does not require forming the "stackable add-on layer" on a second substrate.

That read is inconsistent with the intrinsic record. Although "separately fabricated" is not a disputed term, both the '702 Patent and the '941 Patent use that modifier to refer to separately fabricated base and SOI substrates. *See, e.g.*, '702 Patent at [57] (noting the "[t]he plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which subsequent to attachment [to the base substrate] are etched to produce individual doped stack structures"); *id.* at 1:57–62 (same); '941 Patent at 1:9–12 (noting the invention "relates to combining a semiconductor substrate with a thin add-on semiconductor layer in which various active and/or passive devices have been fabricated"). *See also* '941 Patent at 8:53–10:3 (describing, with respect to Figures 4A–4D, forming doped layers on an SOI substrate 190, bonding the doped layers to a dielectric layer formed on a base substrate 180, and removing the SOI substrate 190 by etching or polishing).

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). Here, the intrinsic record shows "stackable add-on layer" should be construed as "a layer formed separately from the substrate suitable to be bonded to the dielectric layer positioned above the substrate." Given that, a "stackable add-on layer" cannot be a layer formed *in situ* by sequential

deposition on the dielectric layer.

B. "SOI pillar" ('702 Patent, Claims 14–16)

BeSang's Construction	Micron's Construction
Plain and ordinary meaning; no construction necessary. Alternative: "a silicon-on-insulator structure taller than it is wide."	"a doped stack structure formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated wafer or similar type of substrate"

This dispute concerns three dependent claims:

> 14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a **SOI pillar**.
>
> 15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a **SOI pillar**.
>
> 16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first **SOI pillar**.

'702 Patent at 12:35–47 (emphasis added).

The parties present different disputes. BeSang seeks to limit the ratio of the height of the recited "SOI pillar" to its width. Micron, on the other hand, tries to limit "pillar" to how that structure is formed.

1. BeSang's construction

BeSang's expert says a "pillar" is "used in the field of semiconductor devices to describe devices or structures that are relatively taller than they are wide." Glew Decl., Dkt. No. 113-2 ¶ 87. To support that conclusion, he cites several technical papers that describe pillars with dimensions

that align with BeSang's proposal—not that the ordinary meaning of "pillar" in this art *requires* such a relationship. For example, Dr. Glew cites one IEEE article for its description of "pillar" structures having 6 µm or 12 µm heights and 2 µm diameters. *Id.* (citing *Fabrication of Pillar-Structured Thermal Neutron Detectors*, Rebecca J. Nikolic, IEEE 2007, BESANG-MICRON_0004546). He cites another IEEE article that describes silicon "pillar" structures with 20 µm heights and 1.4 and 2 µm diameters. *Id.* (citing *Harvesting and Transferring Vertical Pillar Arrays of Single-Crystal Semiconductor Devices to Arbitrary Substrates*, Logeeswaran VJ, IEEE 2010, BESANG-MICRON_0004537).

In its response, Micron says "the '702 Patent teaches to avoid 'pillar' structures that are taller than they are wide." Dkt. No. 122 at 30 (citing '702 Patent at 9:19–23, 10:35–38). It says BeSang's construction contradicts the patent's teaching of a relatively low effective aspect ratio, "making the pillar vulnerable to toppling." *Id.*

Ultimately, neither party presents a persuasive case for its construction. While it seems intuitive that most of the time an "SOI pillar" would be taller than it is wide, nothing in the intrinsic or extrinsic evidence *requires* that. And while the patent might express a preference for avoiding a "high aspect ratio," it doesn't explain what it means by "high." The Court therefore declines to take a position on the required height-to-width ratio for now.

2. Micron's construction

Micron's construction has two parts: (a) whether the SOI pillar must be a "doped stack structure," and (b) how it is formed.

a. Whether an SOI pillar must be a "doped stack structure"

Micron says the specification defines "pillar." Dkt. No. 122 at 28. Specifically, Micron points to the patent's description that, "[i]n various embodiments of the present invention, a FLD

can be directly contacted by metal electrons at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures)." '702 Patent at 6:26–29. BeSang says this is not lexicography because that excerpt refers to exemplary embodiments. Dkt. No. 113 at 28. And even if it is definitional, it would define "individual doped stack structures" to be "pillar structures"—not the other way around. *Id.* (citing *SkinMedica, Inc. v. Histogen, Inc.*, 727 F.3d 1187, 1200 (Fed. Cir. 2013)).

The Court agrees with Micron. First, although "a patentee's use of 'i.e.' can show an intent to define the word to which it refers," "such use . . . is not absolute." *SkinMedica*, 727 F.3d at 1201. In *SkinMedica*, the claim at issue recited the step of "culturing fibroblast cells in three-dimensions in a cell culture medium." *Id.* at 1190. SkinMedica asserted the claimed three-dimensional culturing could be done using "beads," but the district court concluded the patentees "explicitly defined beads as a two-dimensional culture method" by, among other things, using the phrase "beads (i.e. two-dimensions)." *Id.* at 1193. The appellate court affirmed based in part on the patentee's use of "i.e.," but also noted "[r]eading "beads (*i.e.*, two-dimensions)" as definitional comports with the plain language of the specification as a whole and the inventors clearly expressed intent to differentiate the use of beads from three-dimensional culturing. *Id.* at 1201.

Importantly, however, the Court also noted that "the 'use of two terms as alternatives' functions as a redefinition of a term if that redefinition is 'so clear that it equates to an explicit one.'" *SkinMedica*, 727 F.3d at 1202 (quoting *Thorner*, 669 F.3d at 1368). Here, the patent only uses the phrase "individual doped stack structures" four times. After the paragraph containing the "i.e.," the patent only refers to pillars, and the patent only refers to "doped stack structures" in the figures as "SOI pillar 124." This is consistent with the purpose of the pillars, which is "providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller."

'702 Patent at 1:40–43. Accordingly, the Court holds an SOI pillar is a "doped stack structure."

b. Whether an "SOI pillar" must be "formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated or similar type of substrate"

This also concerns lexicography. Micron points to the patent's definition of "SOI layer" as "a relatively thin, single crystal portion of a semiconductor wafer that can be bonded to another previously fabricated wafer." Dkt. No. 122 at 27 (quoting '702 Patent at 4:47–53). Micron also points to the '941 Patent's explanation that, "[b]ecause single crystalline semiconductor layer 124 is formed by SOI technology, it is referred to herein simply as SOI." *Id.* at 28 (quoting '941 Patent at 6:44–46). BeSang considers Micron's approach cobbling together language from the patent to round out the construction. Dkt. No. 113 at 28.

The Court agrees with BeSang. Unlike the other disputed term, nothing about this term itself suggests a pillar must be formed a certain way other than just using SOI technology. Moreover, Micron has not shown the patent clearly and unambiguously defines "SOI pillar" to limit the way it is formed. Accordingly, the Court rejects that part of Micron's construction.

* * *

Based on the foregoing, the Court construes "SOI pillar" as "SOI doped stack pillar structure."

V. CONCLUSION

Disputed Term	The Court's Construction
"stackable add-on layer" ('702 Patent, Claim 13)	"a layer formed separately from the substrate suitable to be bonded to the dielectric layer positioned above the substrate"
"SOI pillar" ('702 Patent, Claims 14–16)	"SOI doped stack pillar structure"

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party's claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. Neither party may take a position before the jury that contradicts the Court's reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

SIGNED this 4th day of August, 2025.

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE